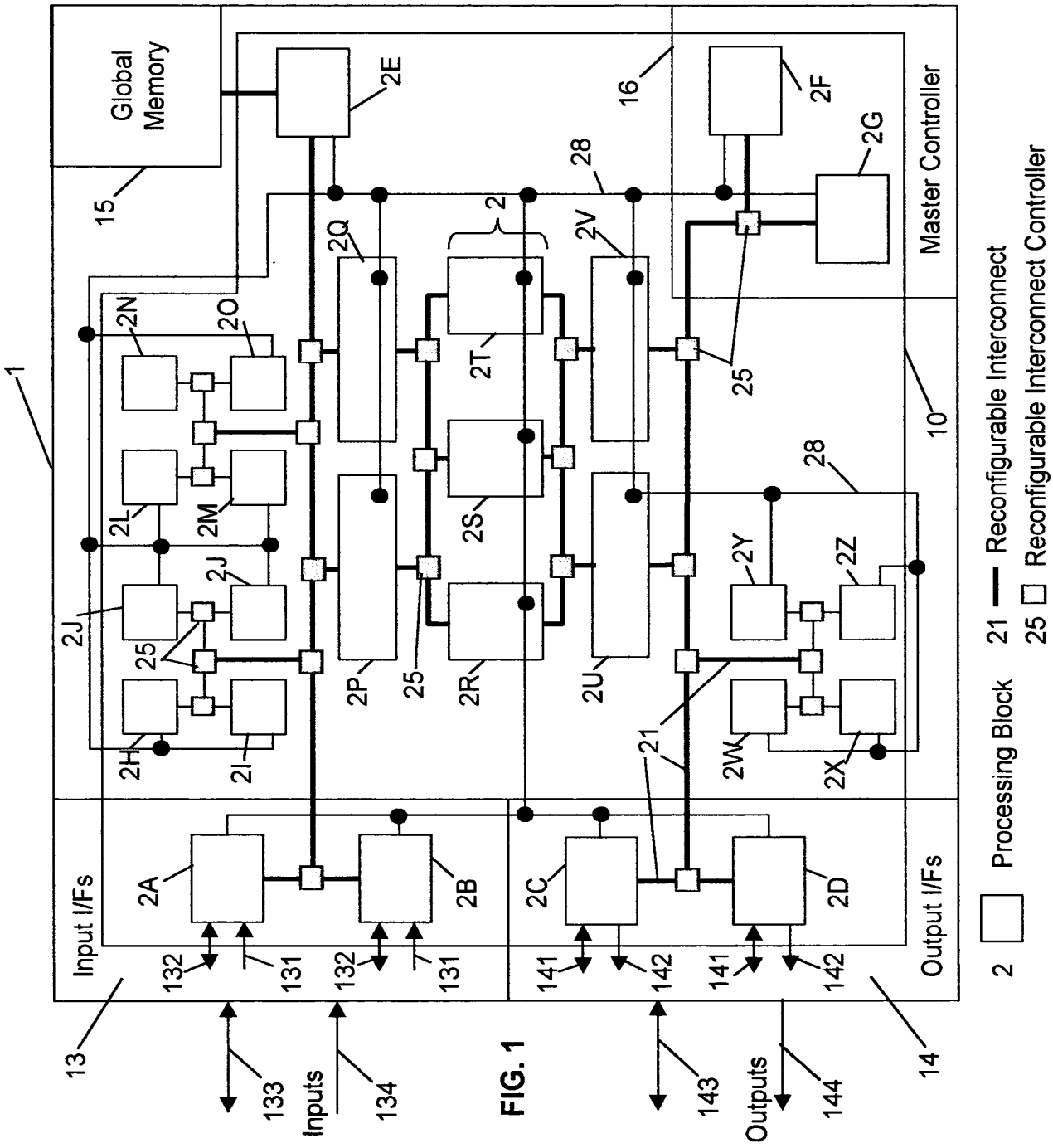

Global Memory
15
Master Controller
16
10
1
Input I/Fs
13
Output I/Fs
14
2A
2B
2C
2D
2E
2F
2G
2H
2I
2J
2L
2M
2N
2O
2P
2Q
2R
2S
2T
2U
2V
2W
2X
2Y
2Z
2
21
25
28
131
132
133
134
141
142
143
144
Inputs
Outputs
2 Processing Block
21 Reconfigurable Interconnect
25 Reconfigurable Interconnect Controller

FIG. 1

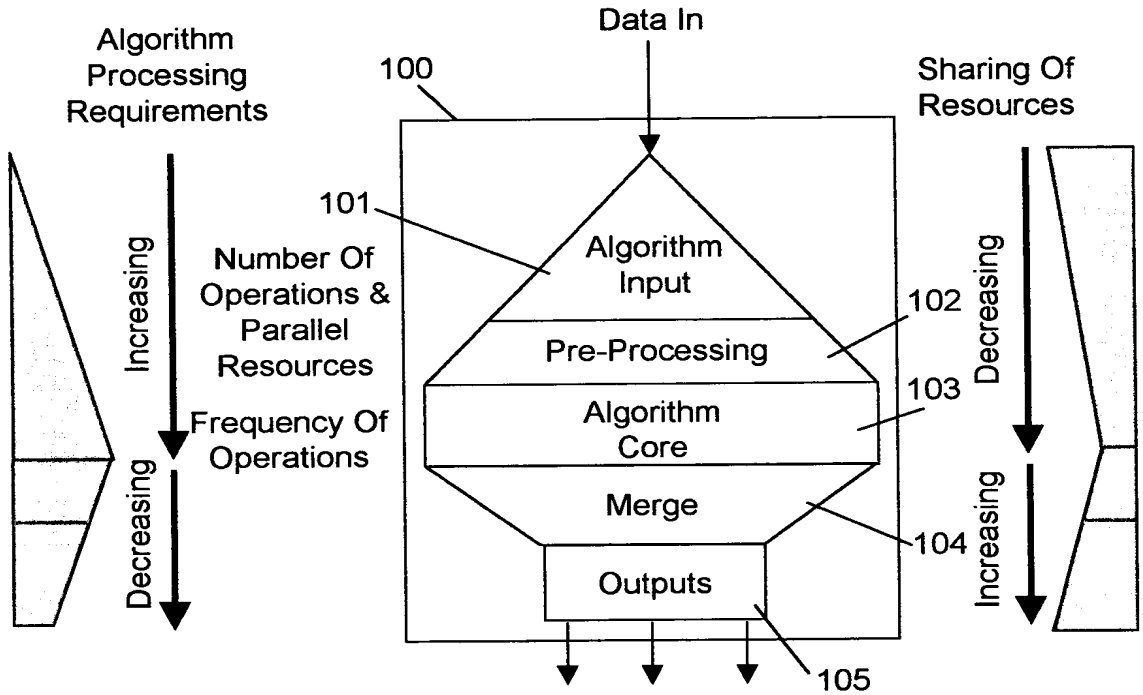

Algorithm Processing Requirements
Increasing
Number Of Operations & Parallel Resources
Frequency Of Operations
Decreasing
Data In
100
101
Algorithm Input
Pre-Processing
102
Algorithm Core
103
Merge
104
Outputs
105
Sharing Of Resources
Decreasing
Increasing

FIG. 2

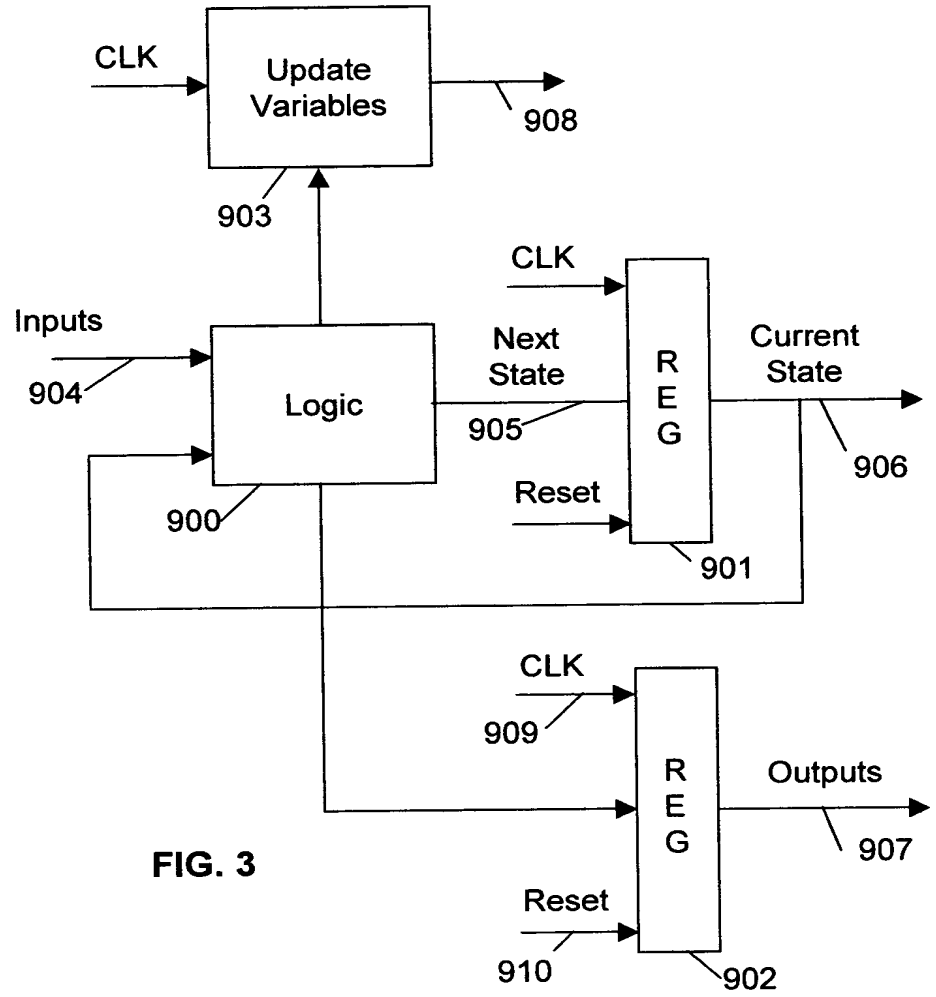

CLK
Update Variables
908
903
CLK
Inputs
904
Logic
Next State
905
R E G
Current State
906
Reset
900
901
CLK
909
R E G
Outputs
907
Reset
910
902

FIG. 3

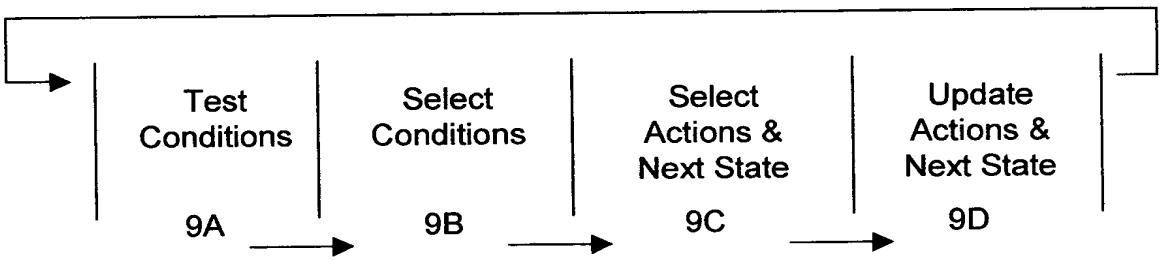
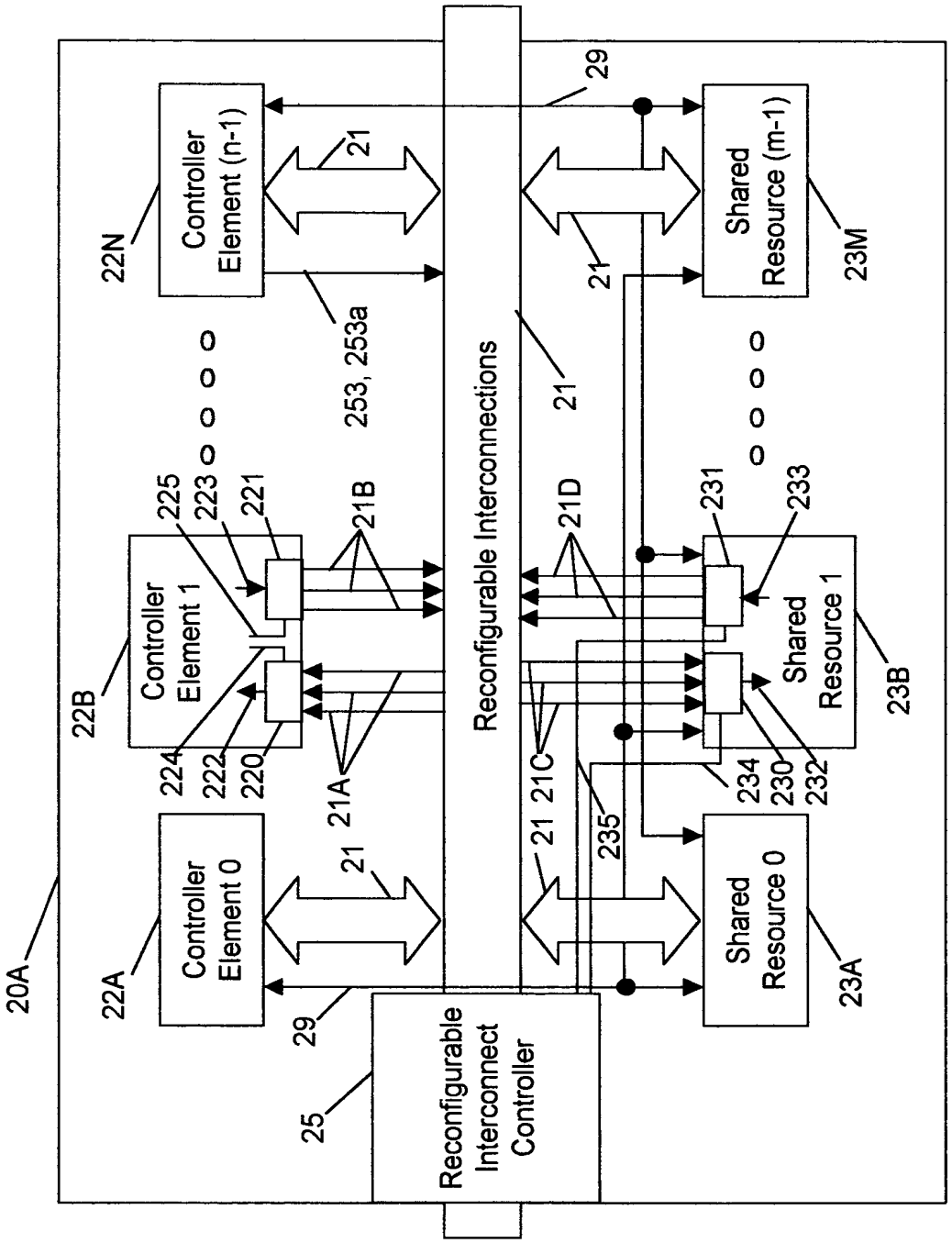

Test Conditions
9A
Select Conditions
9B
Select Actions & Next State
9C
Update Actions & Next State
9D

FIG 4


20A
22N
Controller Element (n-1)
22B
Controller Element 1
22A
Controller Element 0
Reconfigurable Interconnect Controller
25
29
Reconfigurable Interconnections
21
253, 253a
225
223
221
21B
224
222
220
21A
21D
21C
235
231
233
234
230
232
Shared Resource (m-1)
23M
Shared Resource 1
23B
Shared Resource 0
23A

2

FIG. 5

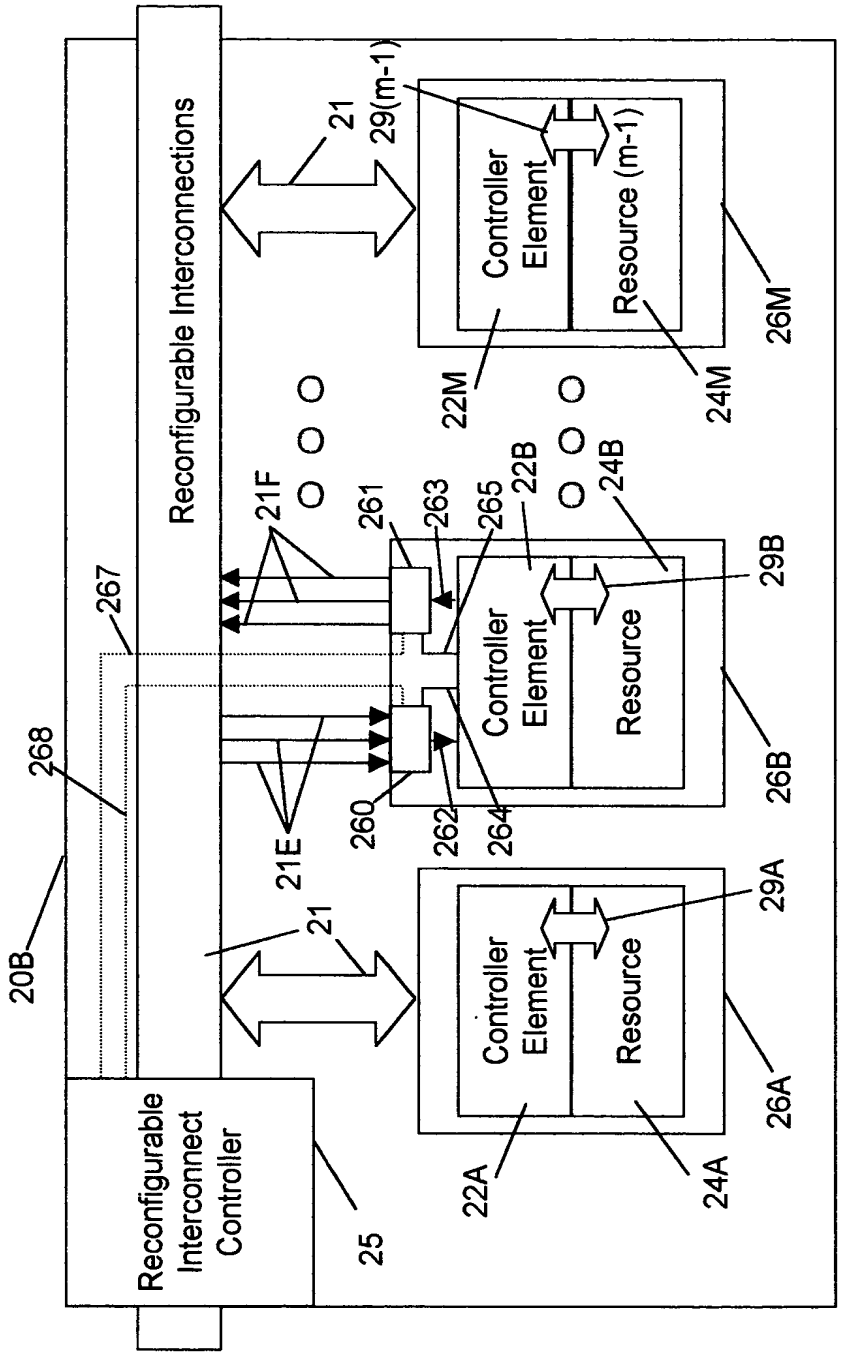

Reconfigurable Interconnections
Reconfigurable Interconnect Controller
Controller Element
Resource
Resource (m-1)
20B
21
21E
21F
22A
22B
22M
24A
24B
24M
25
26A
26B
26M
29A
29B
29(m-1)
260
261
262
263
264
265
267
268
2

FIG. 6

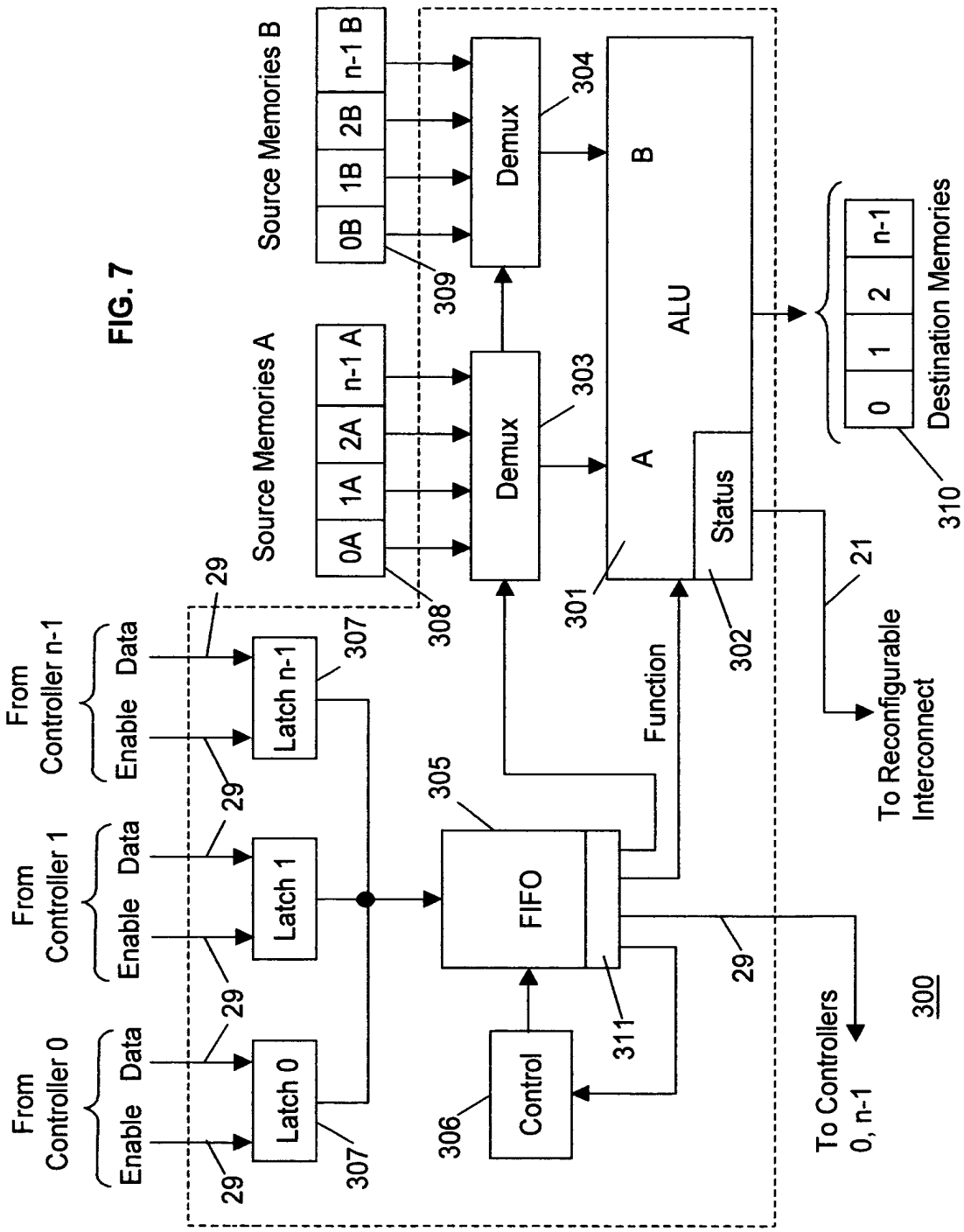

From Controller 0
Enable
Data
From Controller 1
From Controller n-1
29
Latch 0
Latch 1
Latch n-1
307
Source Memories A
0A
1A
2A
n-1 A
308
Source Memories B
0B
1B
2B
n-1 B
309
Demux
303
304
FIFO
305
Control
306
311
Function
ALU
A
B
301
Status
302
21
To Reconfigurable Interconnect
To Controllers 0, n-1
Destination Memories
0
1
2
n-1
310
300

FIG. 7

320

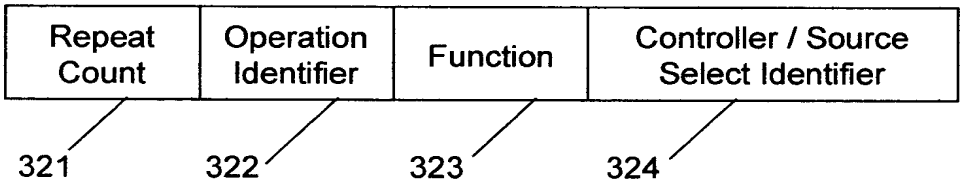

Repeat Count
Operation Identifier
Function
Controller / Source Select Identifier
321
322
323
324

FIG. 8

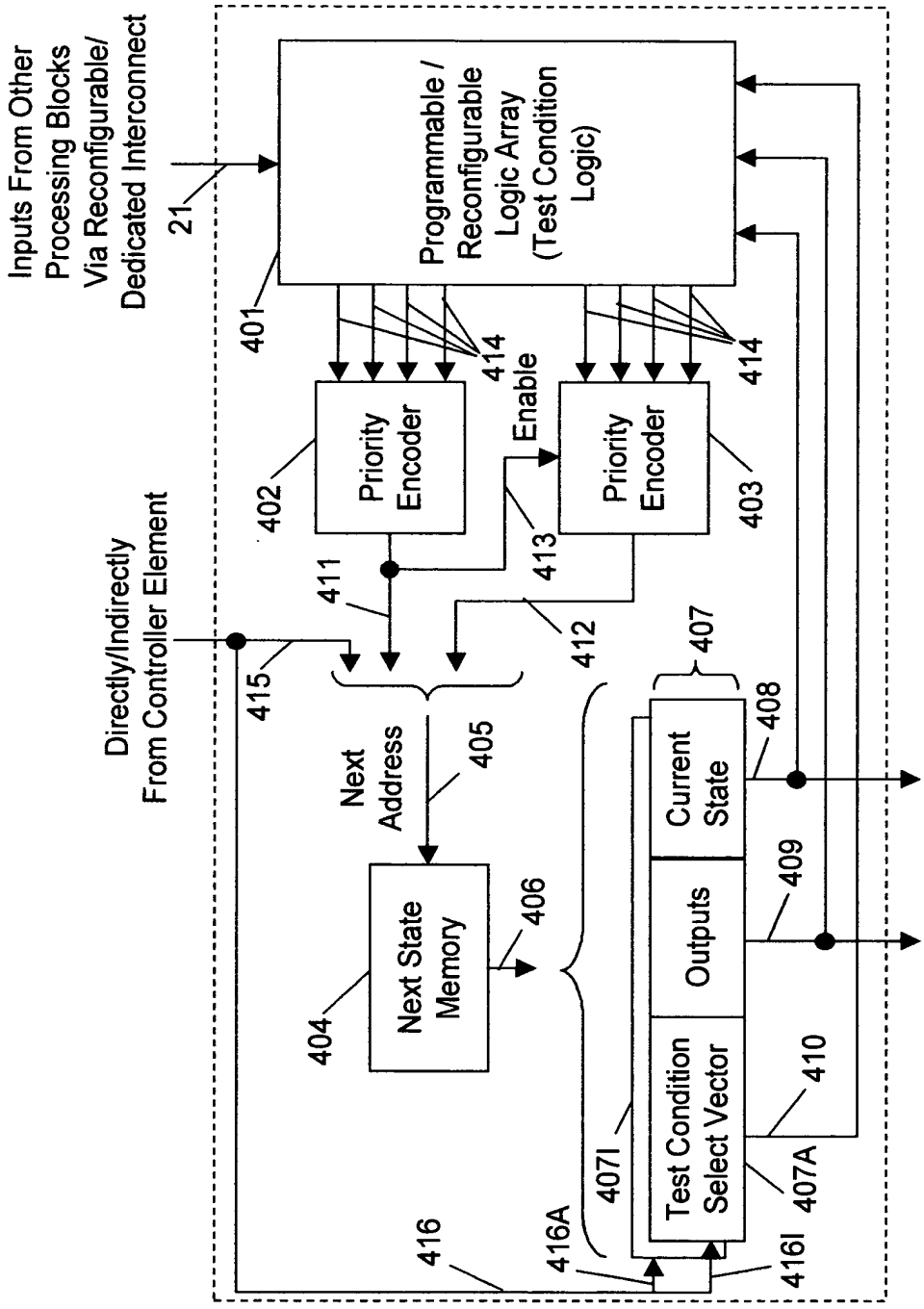

Inputs From Other Processing Blocks Via Reconfigurable/ Dedicated Interconnect
21
Programmable / Reconfigurable Logic Array (Test Condition Logic)
401
414
414
Priority Encoder
402
Enable
413
Priority Encoder
403
411
412
Directly/Indirectly From Controller Element
415
407
Next Address
405
408
Current State
409
Outputs
Next State Memory
406
404
Test Condition Select Vector
410
407A
407I
416A
416
416I
400
Directly/Indirectly To Reconfigurable Interconnect - 21

FIG. 9

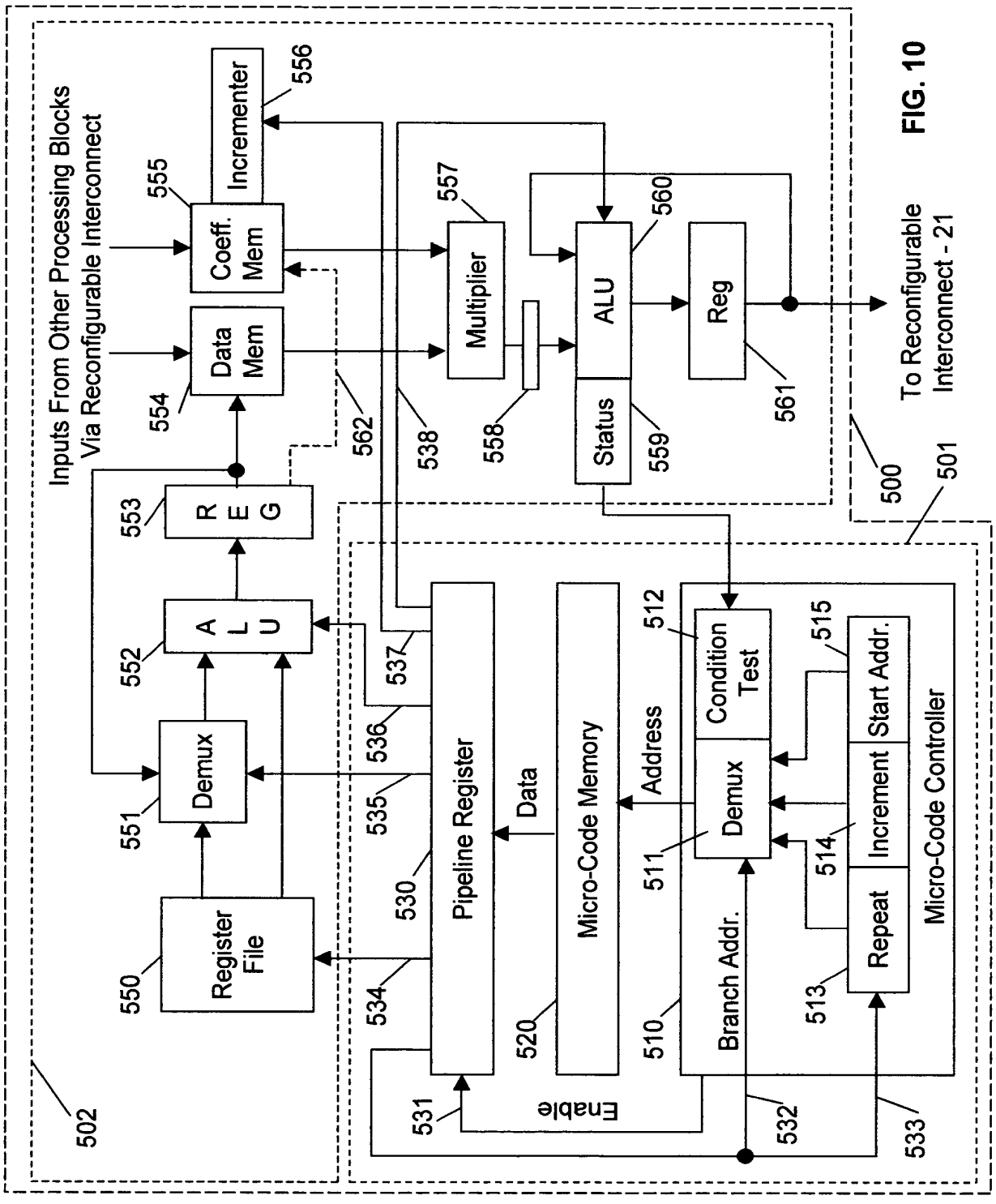

Inputs From Other Processing Blocks
Via Reconfigurable Interconnect
502
501
500
To Reconfigurable
Interconnect - 21
Register
File
550
Demux
551
A
L
U
552
R
E
G
553
Data
Mem
554
Coeff.
Mem
555
Incrementer
556
Multiplier
557
ALU
560
Reg
561
Status
559
562
538
558
537
536
535
530
534
Pipeline Register
Data
Micro-Code Memory
520
Address
Condition
Test
512
Demux
511
Branch Addr.
510
515
Start Addr.
Increment
514
Repeat
513
Micro-Code Controller
Enable
531
532
533

FIG. 10

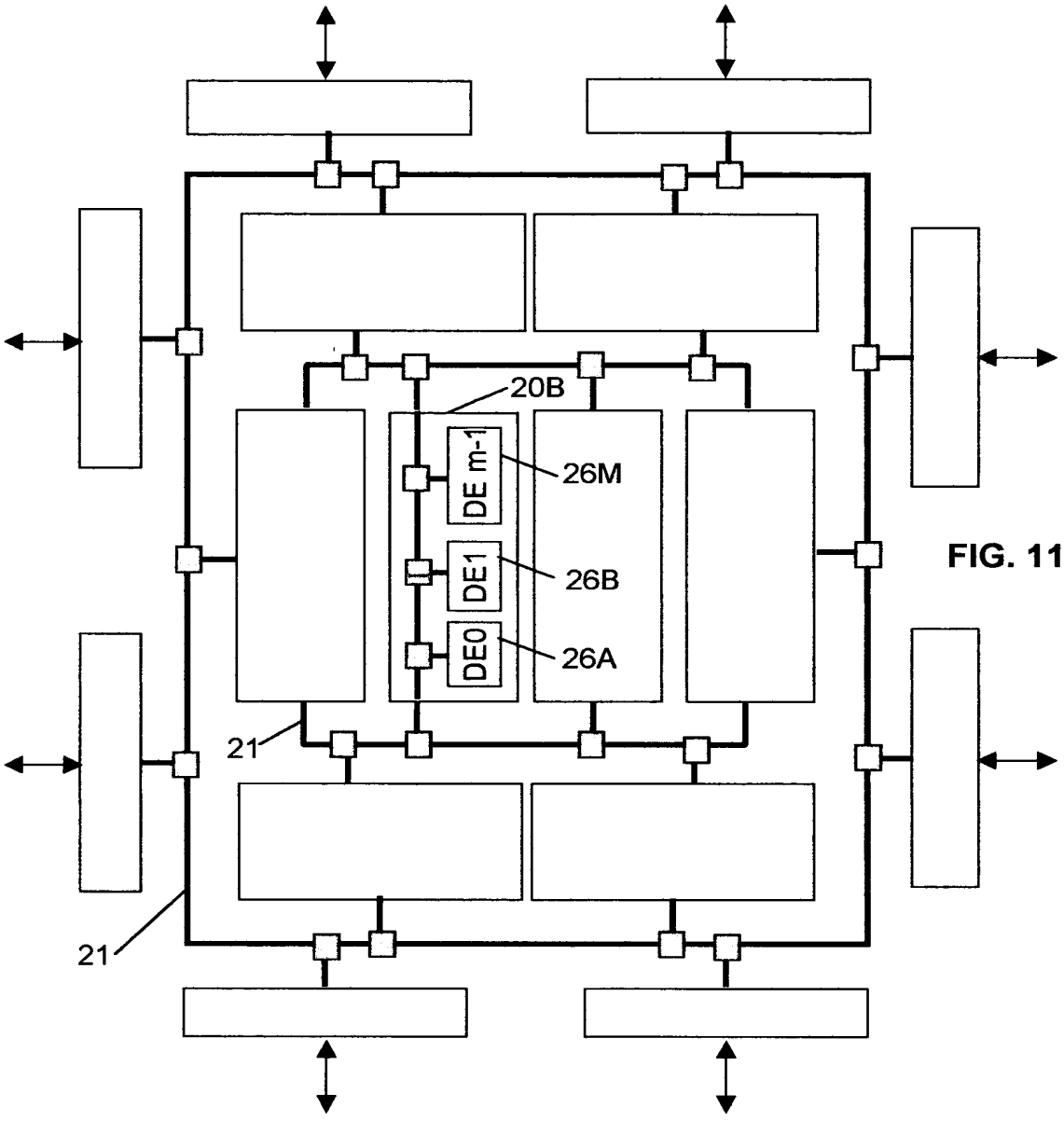


FIG. 11

2 = 20A/20B Dedicated Or Shared Resources

25 Reconfigurable Interconnect Controller

21 Reconfigurable Interconnect

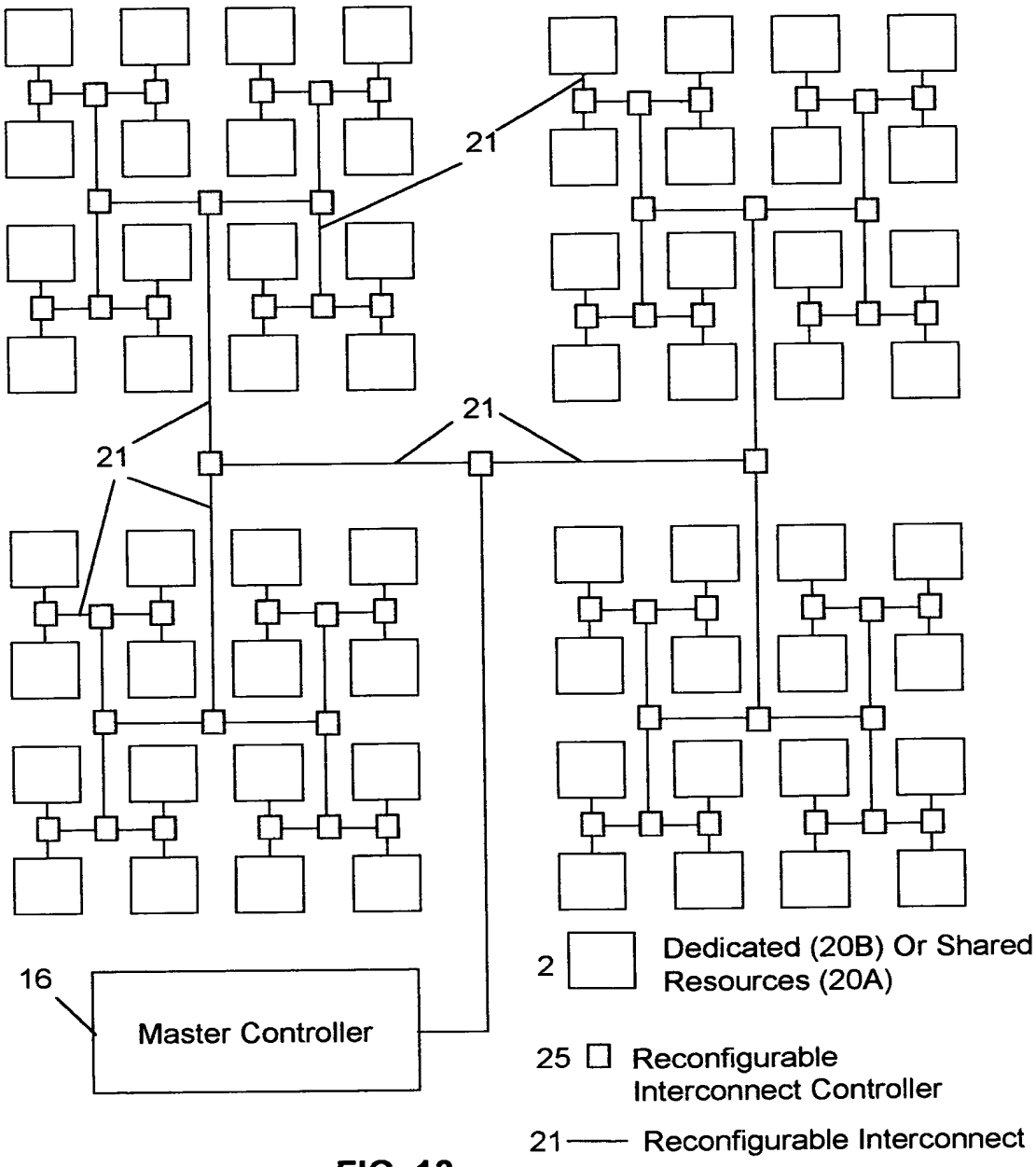

21
21
21
16
Master Controller
2
Dedicated (20B) Or Shared Resources (20A)
25
Reconfigurable Interconnect Controller
21
Reconfigurable Interconnect

FIG. 12

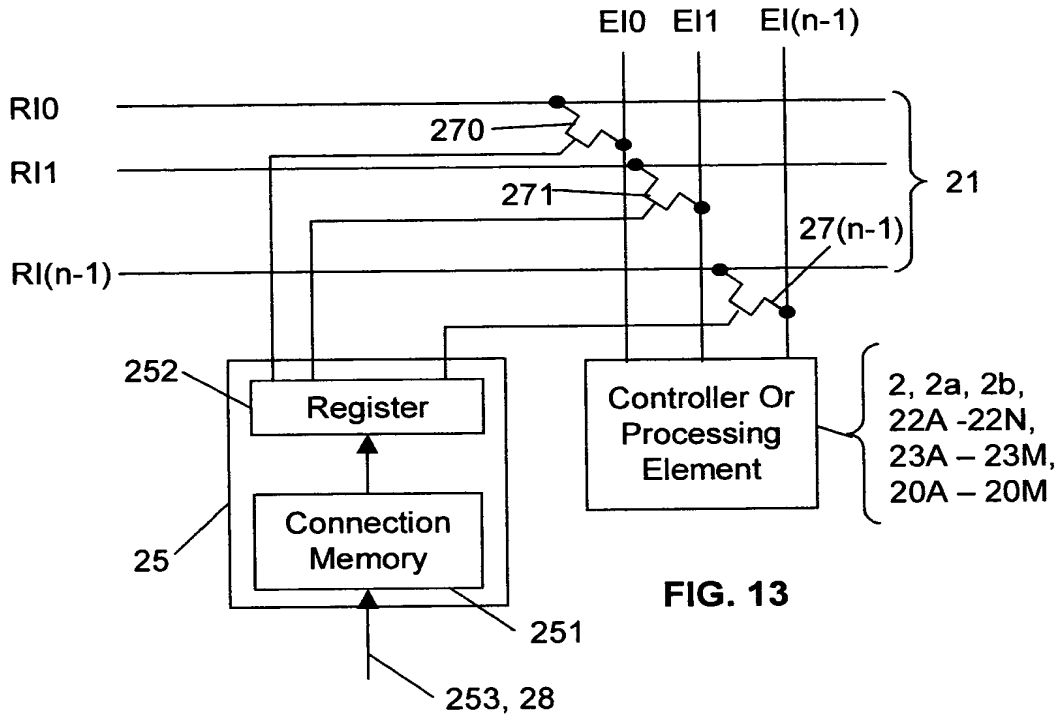

EI0
EI1
EI(n-1)
RI0
RI1
RI(n-1)
270
271
27(n-1)
21
252
Register
Connection Memory
25
251
253, 28
Controller Or Processing Element
2, 2a, 2b,
22A -22N,
23A – 23M,
20A – 20M

FIG. 13

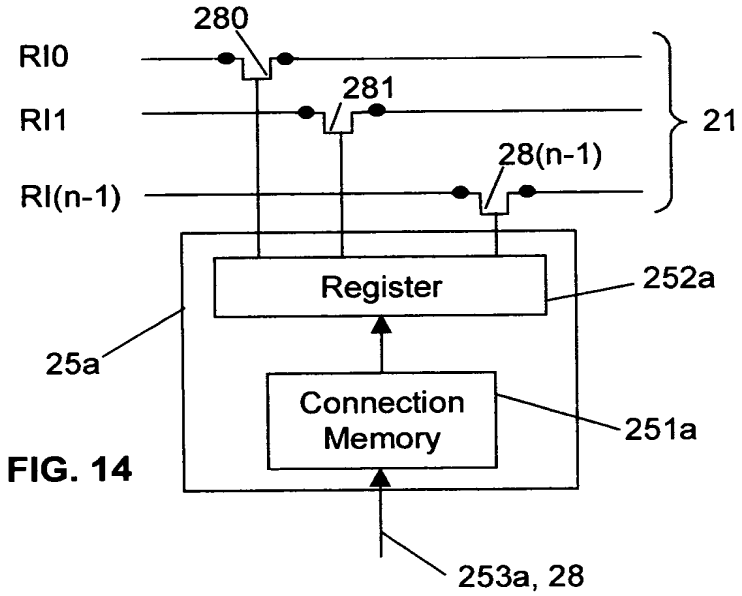

280
RI0
281
RI1
28(n-1)
RI(n-1)
21
Register
252a
25a
Connection Memory
251a
253a, 28

FIG. 14

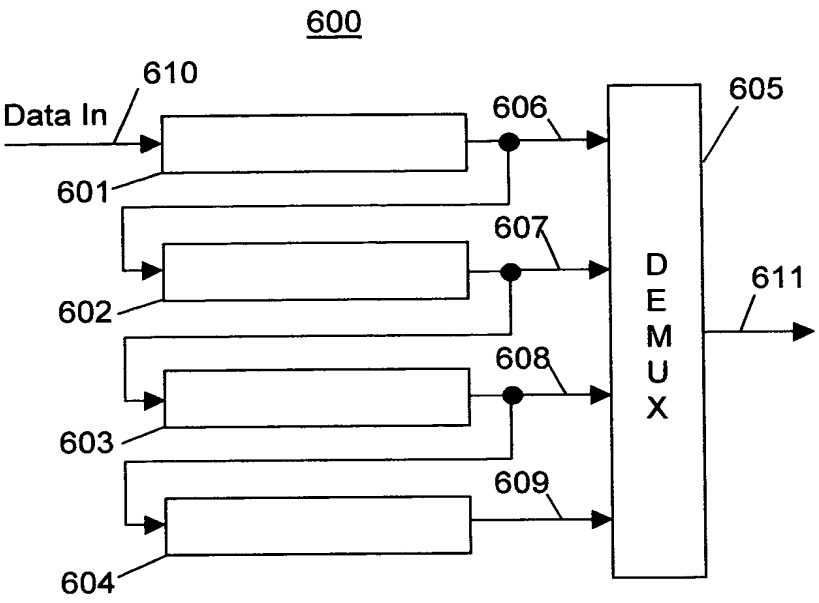


FIG. 15

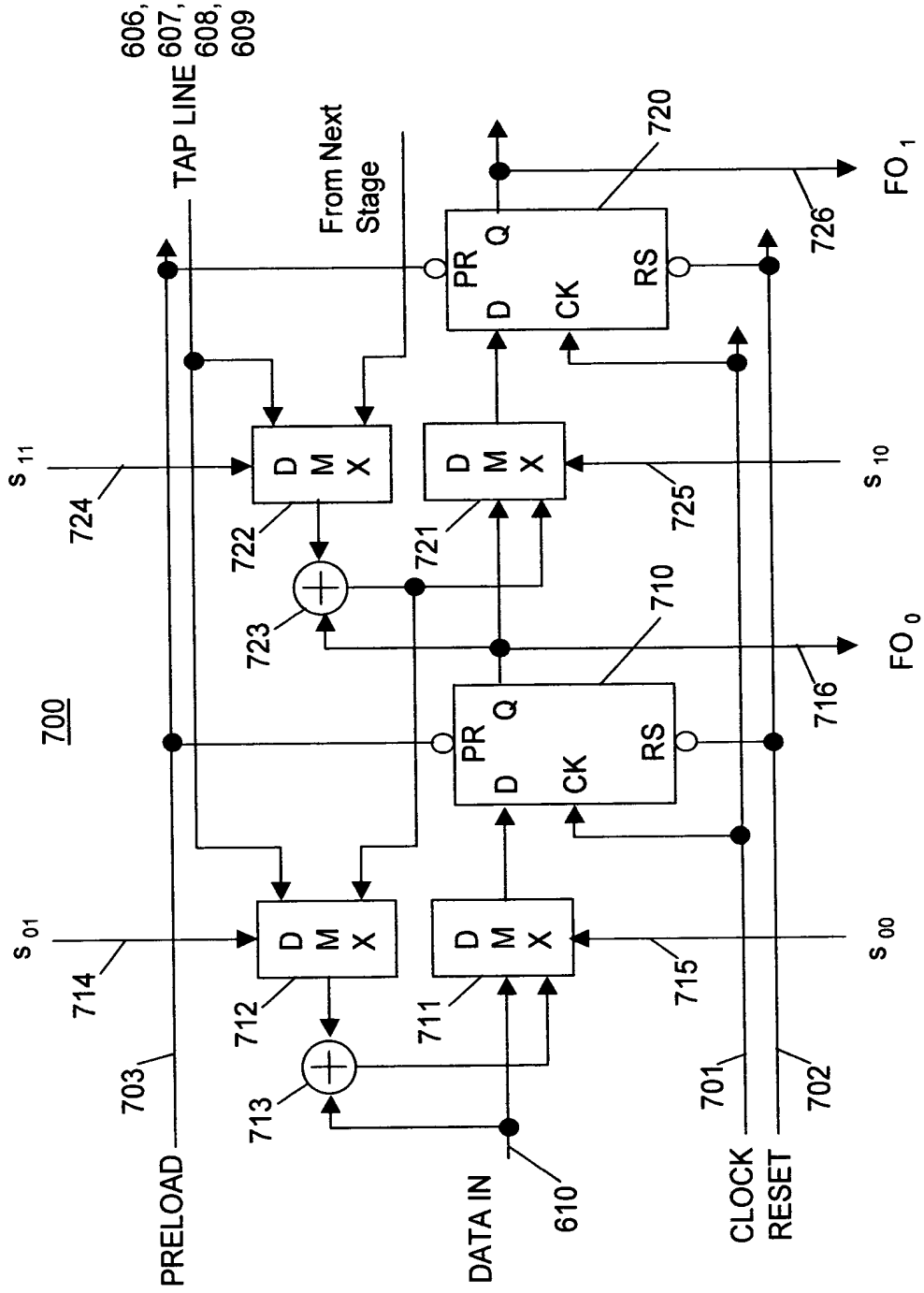

606, 607, 608, 609
TAP LINE
From Next Stage
720
FO 1
726
PR
Q
D
CK
RS
D M X
724
722
721
725
S 11
S 10
723
710
FO 0
716
700
714
712
711
715
S 01
S 00
703
713
701
702
PRELOAD
DATA IN
610
CLOCK
RESET

FIG. 16

AC3 Exponent Decoding Pseudo Code

```
expacc = gexp[i];
dexp[i] = truncate (expacc/25);
dexp[i] = dexp[i]-2;
aexp[i] = prevexp + dexp[i];
prevexp = aexp[i];
```

FIG. 17

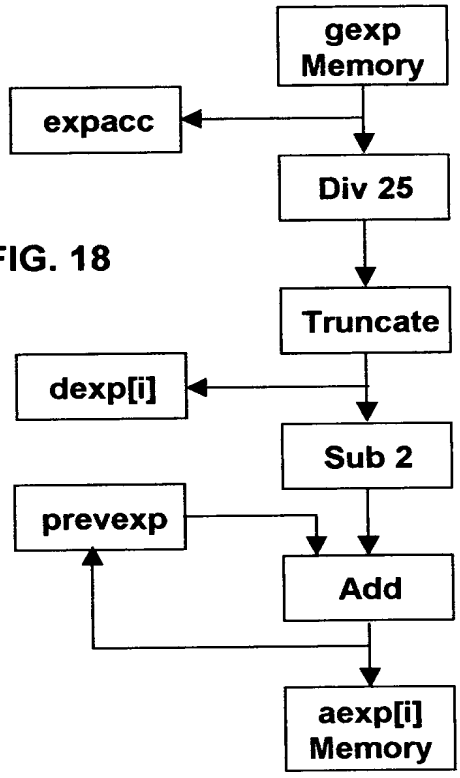


FIG. 18

Routing Configuration Stage [i]

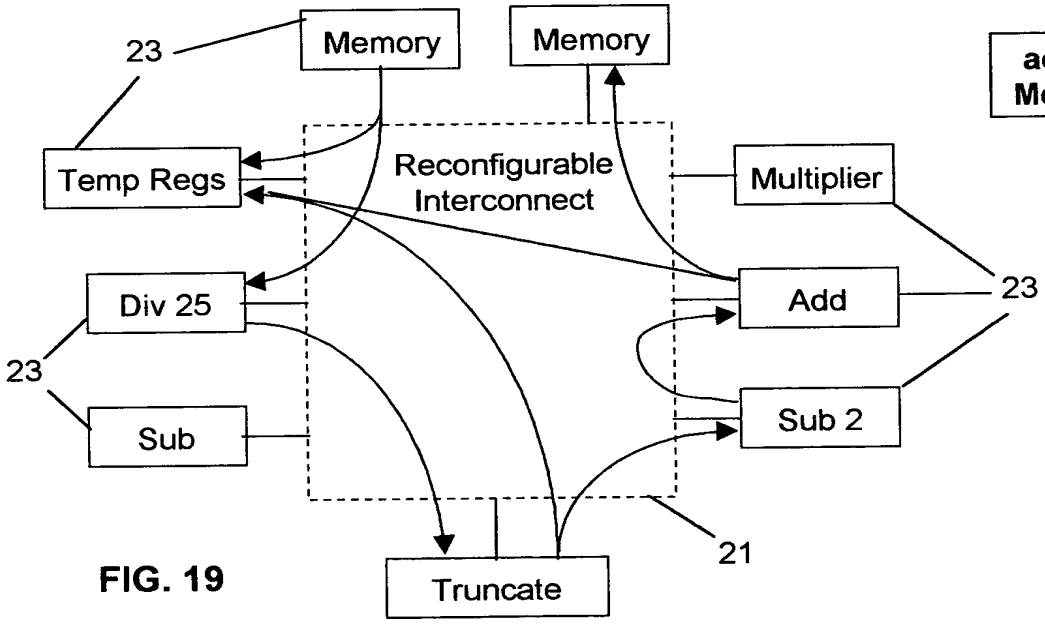


FIG. 19

AC3 Exponent Decoding Pseudo Code

```
expacc = expacc – (25* dexp[i]);
dexp[i+1] = truncate (expacc]/5);
dexp[i+1] = dexp[i+1]-2;
aexp[i+1] = prevexp + dexp[i+1];
prevexp = aexp[i+1];
```

FIG. 20

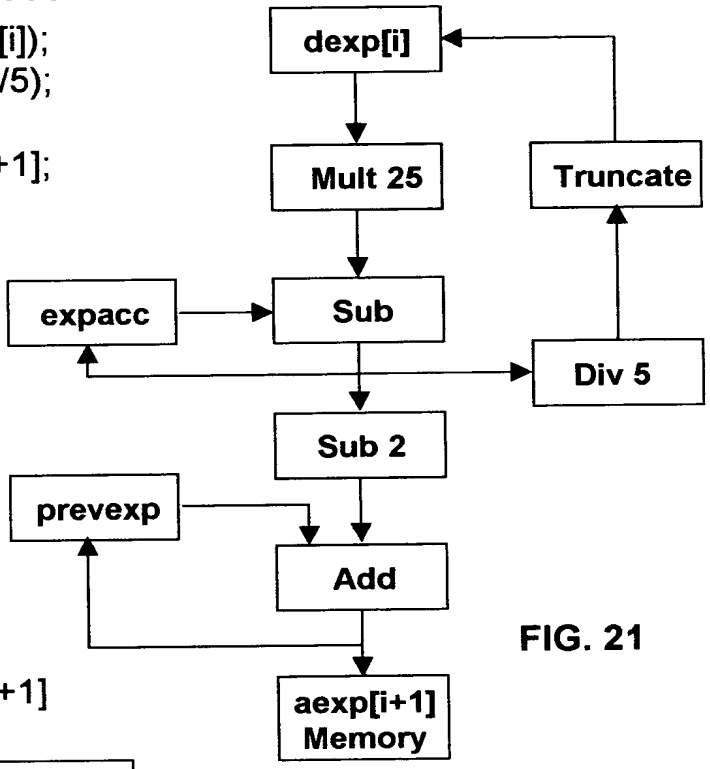


FIG. 21

Routing Configuration Stage [i+1]

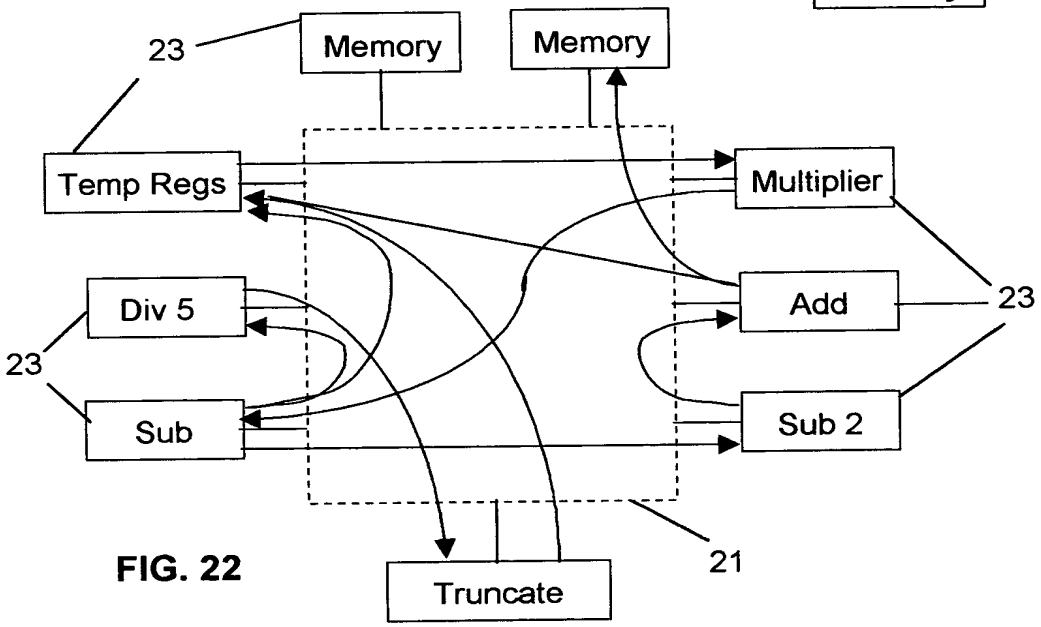


FIG. 22